

REMARKS

Claims 1-12, 14-16 and 18-21 are pending in the present application. By this Amendment, claim 21 is added. No new matter is added. Claims 1-4 and 21 are independent.

Claim Rejections – 35 U.S.C. § 102

Claims 1-12, 14-16 and 18-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Surlekar, USP 5,668,764. This rejection is respectfully traversed.

Surlekar fails to disclose or suggest “a selection circuit for controlling transfer paths of the internal signals and data in response to selection signals, the selection signals corresponding to test information signals” (emphasis added), as recited in claim 1 and similarly recited in claim 3.

Although Surlekar discloses a selection circuit 35 (Fig. 3), it is respectfully submitted that the selection circuit 35 of Surlekar merely discloses receiving only output signals from sense amplifiers 31-34. In other words, Surlekar discloses in response to a local input/output amplifier signal, the data signal from one of the sense amplifiers 31-34 is applied to generate a predetermined data line 36. That is, Surlekar discloses receiving only the data signals, whereas Applicants’ invention discloses the selection circuit controlling the transfer paths of the internal signals and data signals. As an example embodiment, Fig. 2 of the present invention illustrates a selection circuit 120 controlling the internal signals INTSO’-INTS3’ and the data D0-D3.

Further, it is submitted that Surlekar also fails to disclose that the control of the selection circuit is in response to the selection signals. The selection circuit 35 of Surlekar is controlled by data line signals that is compared through comparators 41, 42, 43 from the right top quadrant, left top quadrant, right bottom quadrant, and left bottom quadrant (col. 3, lines 15-26).

Accordingly, Surlekar fails to disclose or suggest a selection circuit for controlling transfer paths of the internal signals and data in response to selection signals, the selection signals corresponding to test information signals, as recited in claim 1.

With regard to claim 2, Surlekar fails to disclose or suggest a second selection circuit for receiving output signals from the first selection circuit and output signals from a sense amplifier, and for opening an alternative one of transfer paths for the internal signals and the output signals of the sense amplifier in response to the selection signals.

The Examiner alleges that “Surlekar teaches a second selection circuit (multiplexer, 47) for receiving output signals from the first selection circuit (35, Figure 3) and output signals from a sense amplifier (33, Figure 3).” However, it is respectfully submitted that the multiplexer 47 is not a second selection circuit. In fact, the multiplexer 47 shown in Fig. 4 of Surlekar discloses that the multiplexer 47 only receives an output signal of an expected data comparison circuit 46 and then outputs a signal to the output buffer 48 (col. 3, lines 39-41). Rather, Applicants’ invention discloses a second selection circuit for receiving output signals from the first selection circuit and output signals from a sense amplifier.

With regard to claim 3, Applicants submit that Surlekar fails to disclose or suggest all of the features recited in claim 3. For example, nowhere does Surlekar disclose selecting a part of internal signals of the integrated circuit device in response to selection signals, the internal signals used for addressing storage locations and for controlling internal operations.

With regard to claim 4, for similar reasons as those stated above with regard to claims 2 and 3, Applicants submit that claim 4 is also allowable over the prior art.

With regard to new claim 21, for similar reasons as those stated above with regard to claim 2, Applicants submit that claim 21 is also allowable over the prior art.

Because Surlekar fails to disclose each and every feature of the claimed invention, it cannot provide a basis for a rejection under 35 U.S.C. §102. Further, Surlekar fails to suggest the claimed invention.

For at least these reasons, Applicants respectfully submit that Surlekar fails to disclose or render obvious the features recited in independent claims 1-4 and 21. Claims 4-12, 14-16 and 18-20, which depend from the respective independent claims are likewise distinguished over the applied art for at least the reasons discussed, as well as for the additional features they recite. Reconsideration and withdrawal of the rejection are respectfully requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the rejections and allowance of each of claims 1-12, 14-16 and 18-21 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKY, & PIERCE, P.L.C.

By 

John A. Castellano, Reg. No. 35,094

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/DJC/cdw